Advanced CMOS Technology 2010 (The 32/22/16 nm Nodes)

3-Day Seminar - October 18, 19, 20 2010 Santa Clara, California

- *Course content is fully updated and current through October-2010*
- *Expanded content includes Logic, Memory (DRAM & Flash) and Analog/RF devices*

1. Detailed process flows for Logic (32nm node), DRAM & Flash
2. Gate-first & gate-last high-k/metal gate integration
3. CMOS device architecture & materials for logic (HP, LP, ULP), memory (SRAM, DRAM, Flash), and Analog/RF/mixed signal applications
4. Mobility enhancement technologies
5. Key process equipment challenges for the 32nm, 22nm, 16nm nodes
6. Copper/low-k integration status & trends
7. Maintaining poly CD control & minimizing process variations
8. Mitigating electrical leakage & implementing power management
9. Lithography: status and future prospects
10. 32nm/22nm/16nm node processing challenges & solutions

Presented by:

This is the one seminar that you need to attend this year to learn about the key technical breakthroughs that have enabled 32nm node technology, and the manufacturing challenges of the 22nm and 16nm nodes

INTRODUCTION:

The relentless drive in the semiconductor industry for smaller, faster and cheaper integrated circuits has brought the industry to the 32 nm technology node. The speed, computational power, and enhanced functionality of ICs based on this advanced technology promise to transform both our work and leisure environments. However the implementation of this technology has opened a Pandora's box of manufacturing issues as well as set the stage for a range of manufacturing challenges that require revolutionary new process methodologies as well as innovative, new equipment for the 22 nm and 16 nm nodes. This seminar addresses all of these manufacturing issues with technical depth and conceptual clarity, and presents leading-edge process solutions to the new and novel set of problems presented by 32 nm node technology, as well as previews the upcoming manufacturing issues of the 22/16 nm nodes.

The central theme of this seminar is an in-depth presentation of the key 32/22/16 nm node technical issues: CD control, electrical leakage mitigation, high-k/metal gate integration, ultra-shallow junction implementation, immersion lithography, mobility enhancement, Copper/low-k integration and other critical processing problems. Each section of the course will present the relevant technical issues in a clear and comprehensible fashion as well as discuss the proposed range of solutions and equipment requirements necessary to resolve each issue.

DETAILED CONTENTS OF SEMINAR TOPICS

1. 32nm node technology at-a-glance – what is different from earlier CMOS technology nodes, and what is the same? What are the key technical issues and roadblocks?
   - Key device and processing concepts: technology node definition, Ion/Ioff curves, scaling methodology
   - The technical driving forces underlying scaling to advanced technology nodes
   - Technical Roadblocks: problems and solutions
   - Unique 32nm/22nm/16nm manufacturing challenges

2. Detailed 32 nm node Logic fabrication Sequence
   - This section of the course presents a detailed step-by-step 32 nm Logic process flow including the FEOL and the BEOL
   - The underlying purpose of each processing operation is discussed and the processing options and equipment considerations for each major module presented
   - Special manufacturing considerations for ultra-small vias and contacts and backend metallization process integration challenges are presented

3. Flash and DRAM device module processing sequences
   - This section of the course presents a detailed step-by-step fabrication sequence for both Flash and DRAM (trench and stacked capacitor)
   - The purpose of each processing step and the fabrication methodology used for each operation are explained in detail.
   - 3D packaging considerations and options are presented

4. Detailed descriptions and striking pictures of state-of-the-art CMOS devices for Logic (High Performance, Low Power, & Ultra-Low Power), Memory (DRAM, SRAM, Flash), and Analog/RF/mixed signal IC applications
   - Brief but technically comprehensive overview of CMOS device structure, function, and materials of construction for all these applications
   - In-depth discussion of all key scaling and functional integration issues for all the applications
   - Detailed device structure and technology roadmaps for all CMOS device applications

5. Why is 32/22/16nm CMOS device technology so sensitive to fabrication process variations? What are the leading-edge fabrication and IC layout/design techniques required to mitigate these yield-killing variations?
   - Root causes of CMOS sensitivity to fab process and layout variations
   - Detailed discussion of all traditional sources of variation (e.g., gate CD, other fab processes)
   - Comprehensive explanation of new "CMOS nanotechnology" variations
   - Techniques that reduce variation in state-of-the-art CMOS

6. The key CMOS problems: leakage and power dissipation- What processing techniques are employed to minimize leakage for low/ultra-low power logic and memory? What power management techniques are effective - how are they implemented? IC applications
   - Leakage suppression techniques for subthreshold, junction, & gate dielectric leakage
   - Power management techniques for active & passive power dissipation

7. Key fabrication process control issues for 32/22/16 nm (and beyond)
   - Lithography/etch process control issues: polygate, contact hole, metal-1 CD control techniques
   - Implant/thermal process control issues: Vt and other parametric variation control techniques
   - State-of-the-art ultra-shallow junction (USJ) formation techniques
   - New sources of process sensitivity/yield impact and appropriate mitigation techniques

8. State-of-the-art CMOS "performance boosters", i.e., mobility enhancement technology - uniaxial strained silicon, substrate orientation, HOT
   - How does strain work to improve carrier mobility and device performance?
   - Leading-edge uniaxial tensile (NMOS) and compressive (PMOS) strain techniques
   - Optimized channel orientation for NMOS & PMOS

9. Lithography update: status and roadmap for state-of-the-art, high volume manufacturing
   - Current status and future prospects for optical lithography
   - Double patterning techniques
   - Future alternatives to optical lithography

10. 22nm, 16nm CMOS roadmap and device technology forecast for all CMOS applications
    - Is the end of bulk, planar CMOS in sight?
    - Key technology forecast issues and "nanoscale" effects - impact on CMOS device architecture/materials
    - The two possible paths forward in CMOS device architecture

SCHEDULE: October 18,19,20 2010
8:00am - 5:00pm daily

LOCATION: Hilton Santa Clara,
4949 Great American Parkway,
Santa Clara California, 95054,
(408) 330-0001

SEMINAR FEE: $1,895

WHAT'S INCLUDED:

a) Three days of instruction by industry experts with in-depth knowledge of the subject material
b) A high quality set of color notes ($495 value) including SEM & TEM micrographs of real-world IC structures that illustrate key technical points
c) Continental breakfast, hot buffet lunch & refreshments served daily

WHO IS THE SEMINAR INTENDED FOR?

- Process Development & Process Integration Engineers & Scientists
- Process Equipment Marketing, Applications, & Product Development Managers, Engineers, & Scientists
- Materials Supplier Marketing, Applications, & Product Development Managers, Engineers, & Scientists
- Process Engineers & Scientists
- Device Engineers & Scientists
- Semiconductor Manufacturing Engineers & Managers
- IC Product Engineering or Marketing Personnel
- VLSI Design Engineers
- Yield & Reliability Enhancement & Failure Analysis Engineers

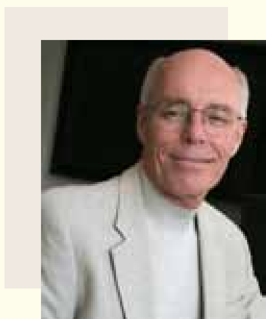
COURSE INSTRUCTORS:

The best instructors in the business will be teaching this course. Both instructors are world-class experts in their respective fields, with decades of industry experience. However, these presenters have been selected not just for their deep technical expertise, but also for their ability to present complex technical information in a clear and engaging manner. Each of these instructors is an experienced and skilled public speaker, and the accompanying course notes for this seminar are profusely illustrated with high-quality color graphics and relevant SEMs and TEMs. It is our intention for you to leave this course with a clear understanding of the key enabling technologies that have made 32 nm node technology a reality and what the central technical challenges are for the 22/16 nm nodes.

Jerry Healey has been a technical professional in the semiconductor industry for over 20 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at the Advanced Technology Development Facility, where he worked on advanced technology node development.

He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, embedded non-volatile memory processing, and mixed signal devices. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

An award winning public speaker, Mr. Healey has taught numerous courses to thousands of practicing engineers and scientists over the past 15 years. He has also authored numerous papers in the field of silicon processing, and is currently the president of Threshold Systems, a firm that provides consulting services and technical training seminars to the semiconductor industry.



Robert Simonton is a widely recognized authority in the subjects of leading-edge CMOS front-end-of-line (FEOL) process integration trends and ion implantation process technology. With over thirty years experience in CMOS device and fabrication technology, Mr. Simonton brings unusual breadth and depth to his lecture topics.

Before 2000, Mr. Simonton has held senior product engineering, advanced product/process development, strategic marketing, and CMOS technology forecasting positions with leading semiconductor process equipment companies such as Varian and Eaton. In January 2000, Mr. Simonton founded Simonton Associates, a semiconductor technology consulting and educational services firm that specializes in resolving high-level product/technology development, technology/marketing management, and IP issues for leading-edge semiconductor IC fabrication companies, process equipment suppliers, and materials suppliers. His consulting and research activities keep him in close touch with key challenges and solutions at each new CMOS technology node.

Mr. Simonton has authored and co-authored over 40 technical papers and four book chapters on semiconductor process technology, and is a recipient of the SRC Outstanding Industrial Mentor Award. He has been a popular lecturer in the field of advanced silicon processing for over 15 years. His audiences remember him for his technical depth, broad industry experience, and his engaging, high-energy lecture style.

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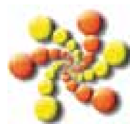

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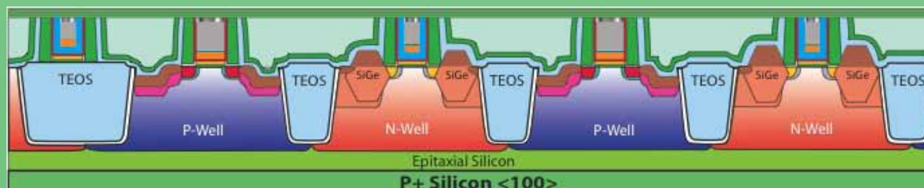

SEMINAR FEE: $1,895

4 WAYS TO REGISTER:

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