JOE STEINBERG

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SUMMARY

Highly effective leader and accomplished Executive with significant global experience in all aspects of operations, management, operations start-up, supply, leadership, government negotiation, and customer interaction. Extensive experience in managing operations in Asia, North and Soutn America, with strong focus on building strong, self-supporting, diverse, cohesive teams resulting in demonstrated success and outstanding measured results. Excellent communicator. Has started up three semiconductor fabrication facilities Motorola in Phoenix Austin and China.

DEMONSTRATED STRENGTHS & ACCOMPLISHMENTS

- Works effectively with international partners and teams.
- ID'd budget and cost for construction and tools, including ship and install at Greenfield China site.
- Executive responsible for pioneering startup of 200mm semiconductor fabrication facility in China, results were **best yielding startup** in history of corporation.
- Negotiated with China government the spin-off of assets for new company, Freescale resulting in ZERO transactional cost and tax-free for five years resulting in savings over $25M.
- Worked on corporate team resulting in new China law, 'Circular 18' creating level playing field and opening up industry for ALL new high technology semiconductor companies operating in China.
- Chairman of Motorola China, Tianjin's General Manager Council, linking all of the businesses together for synergy with customers, costs and manufacturing excellence.
- Significantly lowered customer returns in supply chain for assembly and test semiconductor operation, including unprecedented five consecutive months of zero customer quality incidents.
- Consistently selected diverse, high performing teams at all levels of organization throughout career executing difficult tasks and projects resulting in outstanding operational metrics.

PROFESSIONAL EXPERIENCE

Gordon Pacific llc, Sr Partner **2006-Current**
Asia and US Focus

- Management & Technical consulting for business world wide, extensive experience in Asia and South America
- Cost and operational improvement analysis and implementations.
- Organized renovation, shipment and hookup for new wafer fab in Brazil, including setting up supply chain, hookup team and cost evaluation.
- Produced business plan for South America business park project
- Created plan execution for yield improvement and cost reduction for LCD facility in China
- Valuation and technology analysis for Solar facilities

FREESCALE SEMICONDUCTOR, INC., Austin Texas **1980-2005**
(Formerly Motorola Semiconductor Products Sector (SPS))
Executive Senior Director, Die Manufacturing Operations MOS-11, 2005

- Operations Management for Freescale's highest volume dies production facility.
- Led ramp to full production capacity, initiated additional expansion supporting customer needs.
- Expanded technological capability in RF, SiGe and Power Management to 0.25u.

Motorola
Vice President and General Manager SPS China, 1998-2004
Led negotiation team and developed the negotiation and execution strategy for Freescale spin-off from Motorola.

- Lengthy negotiations involving government from local district to city and state council levels resulting in payment of zero tax including transfer fees, sale taxes and property taxes as a result of the spin-off's asset sale to Freescale. Savings were over $25M.

Directed largest semiconductor assembly and test facility in China

- Operations responsibility for semiconductor assembly and test operations.
- Added cost effective capacity and installed pilot equipment line for Modules
- Increased output from thirty percent in six months.
- Reduced Customer Quality Incidents 65% including 5 months with zero.
- Achieved benchmark OTD metric, >99%.
- Most demanding customer awarded "almost perfect" audit status.

Startup manager for the first 200mm semiconductor wafer mfg facility in China.
Key initiatives included:

- Directly responsible for all aspects executing startup of the first high tech (0.25u) 200mm SMIF, paperless semiconductor wafer manufacturing factory located in China.
- With University of Texas, created home/away MBA curriculum for top 25% high potential engineers to round out and enhance their technical education and training.
- Staffing, team development, recruiting of experienced management and technical team, equipment ID, logistics, installation and qualification, product selection and qualification.
- Government relations and negotiation, licensing permitting were critical aspects of the execution.
- Member of the corporate team negotiation team resulting in new Chinese legislature that became Circular 18. This allowed internationally level playing field for expensive high tech investment in China manufacturing facilities.
- Executed first silicon to schedule with highest yields from any new factory. Outstanding execution allowing removal of 2 cycles of learning from qualification cycletime.
- Qualified new technologies supporting customers with benchmark yields.
- Identified company (SMIC) that purchased wafer factory due to extensive industry downturn.
- Executed creative hiring/training with local Universities for fast learning of complicated processes.

Vice President and Director of Operations Austin Texas, 1992 – 1998

- Strong International interactions with Japan, Hong Kong, Scotland and France
- Directly responsible for high volume manufacturing site.
- Reorganized and revitalized leadership team.

- Upgraded technology almost 5 generations from metal gate to submicron.
- Increased capacity 35% while reducing production costs.
- Consolidated two factories into one ultra high volume low cost facility.

Engineering Management, 1983 - 1992
- Senior Process and Device Engineering Manager.
- Process Engineering Section Manager, Litho, Diffusion, Films and Ion Implant.

Engineer, 1980-1983
- Recruited to Motorola from college as process engineer.
- Process Engineering experience in diffusion, thin films and ion implant.

EDUCATION

BSEE, University of Colorado, Boulder

PUBLICATIONS, PATENTS AND SPEAKING ENGAGEMENTS ADDRESSES

Patents: (3) Epitaxial wafer sealing to prevent autodoping,
Poly Deposition process to minimize shared-contact resistance
Defining a polysilicon capacitor using Ion Implant techniques,
Novel die singulation technique for QFN and MAPBGA packages (pending)

Publications: (8) Gate oxide integrity, Defect reduction, Organizational effectiveness in defect reduction

Journals: Electrochemical Society, Semiconductor International, Sematech